**Title: Phase Synchronization System**

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**Terminology**

In this document the following terminology is used:

PSD. Phase Switching Device. It means any device able to change the characteristics of the input signal to the backend, i.e. switching the pointing in the sky (wobbler or chopper wheel), switching between ambient temperature and the sky (bolometer skydip chopper), switching the received frequency (frequency switching), switching the polarity of the received frequency (polarimeter), or other.

PSS. Phase Switching System. It means the interface (hardware and software) that receives the synchronization signals from all the possible PSDs, selects only one PSD as enable and process its synchronization signals to produce the necessary signals to synchronize the data acquisition.

phase. It means the time with equal characteristics of the signal received. It consists of an initial blanking time to guarantee that the signal is stable and an integration time with useful astronomical information. After the integration time, at the start of the following phase, the integrated signal of the previous phase is recorded.

cycle. It means the minimum sequence of phases that continuously repeat. In a cycle only one phase is the reference of the repetitive sequence of phases. One cycle has one or more phases.

## Introduction

During observations, the signals delivered by the receivers in the Front End (FE) system to the different backends in the Back End (BE) system have fluctuations due to the atmosphere and the receivers. To suppress these undesirable fluctuations different kind of PSDs ( wobbler, chopper, frequency switching,...) are used.

The PSD makes changes of the signal received. Typical ways of producing changes of the signal are: changing the pointing, frequency, polarity or other characteristic of the beam. The BE must be synchronized to integrate the FE data during the integration time of the phase, separating the data from consecutive phases. Depending on the PSD used, two or more phases should be produced per cycle and several cycles complete an astronomical observing subscan. During a subscan all the cycles must be delivered by the same PSD.

Other times the signal is the same in the whole subscan but what is necessary is to resolve the data in time within the subscan. For those cases is necessary to generate artificial phases to resolve the acquired data as a function of the time and the cycle will consists in only one phase.

Finally, if neither different phases are produced nor resolution in time is necessary, we still could not record during the whole subscan because the V/F counters could be saturated due to the possible excesive duration of the subscan. Then the subscan time must be cut into shorter phases of time. The cycle will have also only one phase.

The PSS is in charge to synchronize the data acquisition in the BE system according to the phase switching produced by the PSD selected.

## Operation

The PSD selected must deliver two input signals, *blanking* and *status*, to the digital input module of the PSS, these signals must be TTL level. The output module of the PSS delivers to the BE system three output signals, *Phase Interrupt*, *Status Interrupt* and *Blanking*.

The signals level for the case of a PSD with three phases per cycle is represented in the graphic below. Cycles with three phases are very unusual but has been chosen for clarity of the interpretation. It is more usual cycles with two or four phases.

The first phase of the cycle (phase 1) corresponds to the reference phase. The rising edge of the *blanking* signal always triggers the *Phase Interrupt*. The falling edge of the *blanking* signal is used to check the level of the *status* signal and if the level is high an *Status Interrupt* will be produced at the start of the following phase (phase 2 in the example), indicating that the phase before was the reference phase. The *status* signal must be well defined just at the time of the falling edge of the *blanking* signal, at any other time its level does not care.

The *Blanking* output signal is just a copy of the *blanking* input but with the sense inverted. The *Blanking* output signal is active when the level is low. With the PSD Internal generator the blanking pulse lasts 100 µsec. (in OS9 was 185 µsec.)

In the drawing below the *blanking* and *status* inputs are positive sense, but it is possible to select by software a negative sense if required.

The *Phase Interrupt* output is a negative pulse of 10 µsec. (**IDR**=$500) indicating the starting of any phase (in OS9 was 20 µsec.). This interrupt is generated at the beginning of all the phases.

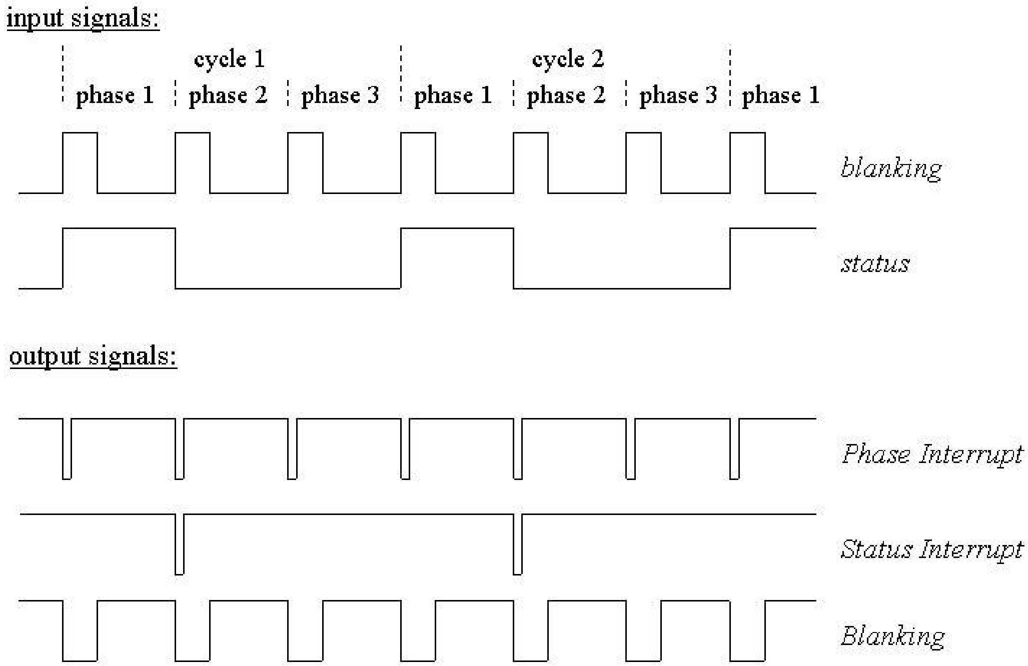
The *Status Interrupt* output is a negative pulse of 10 µsec. (**IDR**=$500) indicating the starting of the phase but just after the reference one (in OS9 was 20 µsec.). This interrupt is generated only during the phase just after the reference one.

The *Blanking* output is a negative signal with a duration determined by the *blanking* input signal.

It is possible to work with PSDs which deliver only the *status* signal and not the *blanking* one. In that case the cycle must have two phases and the rising and falling edges of the *status* signal will be used to trigger the output interrupts. A minimum output *Blanking* signal of 100 µsec. (in OS9 was 185 µsec.) duration will be produced. This minimum blanking is necessary to permit the load and clear of all the BE counters guaranteeing that all the channels integrate the same duration.

If a new PSD is installed at the 30m as a visitor equipment, it must deliver the *blanking* and *status* input signal (or at least the *status* input signal) as described above.

If a new BE system is brought at the 30m as a visitor equipment, it must be able to receive the *Phase Interrupt*, *Status Interrupt* and *Blanking* output signals delivered by the PSS to synchronize the data acquisition.




**Hardware Implementation**

All the PSDs which can be used at the observatory have their *blanking* and *status* signals connected to the PSS. The PSS must be configured by software to select the input signals from only one PSD.

The PSS is hardware implemented with the following VME modules:

1 CPU, model MVME 2401 from Motorola
2 base boards for M-modules, model 201S from MEN
5 M-modules, model M58 from MEN
1 M-module custom designed for the interrupt generation
1 memory module CM-MEM-20

The CPU MVME 2401 runs with the Motorola POWERPC processor under the operating system Linux running in real time. From the startup file in /nfsclients/roots/vac5/etc/rc.d/rc.local the registers are configures and the interrupt routine started. The CPU uses 6 registers (VME memory positions) of 16 bits (words) to configure the operation, 8 registers of 32 bits (longwords) to write the frequency values and 4 tables of up to 64 registers for frequency switching operation. The base address BA for the registers is at the position 0x100000.

The first 201S base board houses the following two M-modules.

The first M-module (third position starting from the bottom) is a M58, 32 bits TTL I/O, at address $C02400, the first 16 bits (ports A and B) are configured as digital inputs and the last 16 bits (ports C and D) are configured as digital outputs. The cable connection of the signals from the PSD to the orange cable interface is according to the following table:

| pin | Bit | signal | pin | Bit | Signal |
|---|---|---|---|---|---|
| 1 | port A, 0 | blanking, beam switching | 2 | port A, 1 | status, beam switching |
| 3 | port A, 2 | blanking, wobbler | 4 | port A, 3 | status, wobbler |
| 5 | port A, 4 | blanking, reserve 1 | 6 | port A, 5 | status, reserve 1 |
| 7 | port A, 6 | blanking, reserve 2 | 8 | port A, 7 | status, reserve 2 |
| 9 | port B, 0 | blanking, reserve 3 | 10 | port B, 1 | status, reserve 3 |
| 11 | port B, 2 | blanking, reserve 4 | 12 | port B, 3 | status, reserve 4 |
| 13 | port B, 4 | out of lock Rx 1 | 14 | port B, 5 | out of lock Rx 2 |
| 15 | port B, 6 | out of lock Rx 3 | 16 | port B, 7 | out of lock Rx 4 |
| 17 | port C, 0 | phase interrupt signal | 18 | port C, 1 | phase interrupt signal |
| 19 | port C, 2 | status interrupt signal | 20 | port C, 3 | status interrupt signal |
| 21 | port C, 4 | blanking signal | 22 | port C, 5 | blanking signal |
| 23 | port C, 6 | blanking wobbler simul. | 24 | port C, 7 | status wobbler simul. |
| 25 | port D, 0 | | 26 | port D, 1 | |
| 27 | port D, 2 | | 28 | port D, 3 | |
| 29 | port D, 4 | | 30 | port D, 5 | |
| 31 | port D, 6 | | 32 | port D, 7 | |
| 33 | | +5V | 34 | | Ground |

The second M-module (fourth position starting from the bottom) is a custom designed module at address $C02600. It generates the VME interrupts to the CPU at the rate 10000 per second. The value of the interrupt vector is 135 and the interrupt level is 5.

The second 201S base board houses four M-modules of the type M58, 32 bits TTL I/O. The base address of this mother board is at address $C03000 and the four M58 are configured as 32 bits digital output. Each M58 controls the synthesizer of the second reference frequency of one receiver, then up to four receivers can be controlled. By means of these four modules the frequency switching is implemented in up to four receivers.

The 32 bit programming of the M-module M58 to synthesize a frequency in the ADRET 90/120 MHz synthesizer is as follow.

| bit | freq. (Hz) | bit | freq. (Hz) | bit | freq. (Hz) | bit | freq. (Hz) |
|---|---|---|---|---|---|---|---|
| 1 | $1 \times 10^1$ | 9 | $1 \times 10^3$ | 17 | $1 \times 10^5$ | 25 | $1 \times 10^7$ |
| 2 | $2 \times 10^1$ | 10 | $2 \times 10^3$ | 18 | $2 \times 10^5$ | 26 | $8 \times 10^7$ |
| 3 | $4 \times 10^1$ | 11 | $4 \times 10^3$ | 19 | $4 \times 10^5$ | 27 | $1 \times 10^8$ |
| 4 | $8 \times 10^1$ | 12 | $8 \times 10^3$ | 20 | $8 \times 10^5$ | 28 | NC |
| 5 | $1 \times 10^2$ | 13 | $1 \times 10^4$ | 21 | $1 \times 10^6$ | 29 | NC |
| 6 | $2 \times 10^2$ | 14 | $2 \times 10^4$ | 22 | $2 \times 10^6$ | 30 | NC |
| 7 | $4 \times 10^2$ | 15 | $4 \times 10^4$ | 23 | $4 \times 10^6$ | 31 | NC |
| 8 | $8 \times 10^2$ | 16 | $8 \times 10^4$ | 24 | $8 \times 10^6$ | 32 | NC |

**Software Implementation**

The PSS is implemented in the "vac5" system at the internet address 150.214.224.196, which run under the Linux operating system. With the PSS process running, one VME interrupt is serviced by the CPU program. The VME interrupt is generated by the custom designed M-module every 0.1 msec. and works as an internal time counter and triggering the polling of the *blanking* and *status* input signals from the selected PSD.

Programs that must be run during the boot to configure the registers and to load the interrupt are:

$ */home/penalver/BESYNC/config*
$ */sbin/modprobe besync*

other useful programs are:

$ */home/penalver/BESYNC/biconf* ! to read and write the registers
$ */home/penalver/BESYNC/freqset* ! to read and set the frequencies

The program *freqset* permits, in an easy way, to work with the frequencies used by the *besync* interrupt application. Frequencies values can be written in MHz and the program converts them to VME data. *freqset* also fills the table of frequencies for frequency switching in ramp mode. With the option "0 1" the values written in the local table are transfered to the VME registers, including the table for frequency switching in ramp mode. *freqset* only permits a maximum value for BTR of 127 (12.7 msec.), this upper limit is mandatory for frequency switching in ramp mode, but not for the other switching configurations.

The application uses 14 registers at the base address BA = $100000 for interfacing with external processes. The application also uses four tables (one table per receiver) with the frequency values used during the blanking time in frequency switching ramp mode. The registers and tables used are resumed in the following table:

| **Address** | **Size** | **Name** | **Full Name** |
|---|---|---|---|
| BA+0x00 | 2 bytes | **STR** | **ST**atus **R**egister |
| BA+0x02 | 2 bytes | **OLR** | **O**ut of **L**ock **R**egister |
| BA+0x04 | 2 bytes | **PTR** | **P**hase **T**ime **R**egister |
| BA+0x06 | 2 bytes | **BTR** | **B**lanking **T**ime **R**egister |
| BA+0x0A | 2 bytes | **LER** | **LE**vel **R**egister |
| BA+0x0E | 2 bytes | **IDR** | **I**nterrupt **D**uration **R**egister |
| BA+0x10 | 4 bytes | **F11** | **F**requency **1** of Rx **1** |
| BA+0x14 | 4 bytes | **F12** | **F**requency **2** of Rx **1** |
| BA+0x18 | 4 bytes | **F21** | **F**requency **1** of Rx **2** |
| BA+0x1C | 4 bytes | **F22** | **F**requency **2** of Rx **2** |
| BA+0x20 | 4 bytes | **F31** | **F**requency **1** of Rx **3** |
| BA+0x24 | 4 bytes | **F32** | **F**requency **2** of Rx **3** |

| | | | |
|---|---|---|---|
| BA+0x28 | 4 bytes | **F41** | **F**requency **1** of Rx **4** |
| BA+0x2C | 4 bytes | **F42** | **F**requency **2** of Rx **4** |
| BA+0x200 | 0x200 bytes | **FS1** | starting table for **FS**, Rx**1** |
| BA+0x400 | 0x200 bytes | **FS2** | starting table for **FS**, Rx**2** |
| BA+0x600 | 0x200 bytes | **FS3** | starting table for **FS**, Rx**3** |
| BA+0x800 | 0x200 bytes | **FS4** | starting table for **FS**, Rx**4** |

Below there is a description of the registers above.

BA+0x00, **STR** (word), **ST**atus **R**egister. It selects the PSD which supplies the *blanking* and the *status* input signals. It selects also if only the *status* input signal is present without *blanking*. The bit use is as follow:

| bit | meaning |
|---|---|
| 1 | enables the internal generator (internal PSD) |
| 2 | enables the frequency switching in jump mode (internal PSD) |
| 3 | enables the frequency switching in ramp mode (internal PSD) |
| 4 | enables the beam switching (external PSD) |
| 5 | enables the wobbler (external PSD) |
| 6 | enables the reserve 1 (external PSD) |
| 7 | enables the reserve 2 (external PSD) |
| 8 | enables the reserve 3 (external PSD) |
| 9 | enables the reserve 4 (external PSD) |
| 10 | free |
| 11 | free |
| 12 | when set only the *status* signal is considered for the cases bit 3 to 8 |
| 13 | enables *Blanking* output with out of lock of Rx 1 |
| 14 | enables *Blanking* output with out of lock of Rx 2 |
| 15 | enables *Blanking* output with out of lock of Rx 3 |
| 16 | enables *Blanking* output with out of lock of Rx 4 |

BA+0x02, **OLR** (word), **O**ut of **L**ock **R**egister. In the **STR** must be set the bits to enable the receivers out of lock, then in case that the corresponding bit in the portB input register shows a level high, the blanking output signal is set (while the input bit in portB is set) and the corresponding bit of the **OLR** is set. Bits of the **OLR** must be set only by the PSS process and reset by the BE process after reading the status. The bit allocation is the following:

bit 0, out of lock status of Rx 1 (if enable)
bit 1, out of lock status of Rx 2 (if enable)
bit 2, out of lock status of Rx 3 (if enable)
bit 3, out of lock status of Rx 4 (if enable)

BA+0x04, **PTR** (word), **P**hase **T**ime **R**egister that defines the phase duration in units of 0.1 msec. with the internal PSDs (internal generator or frequency switching). The minimum value is 2 (0.2 msec.) and the maximum value is 65535 (6.5535 seconds)

BA+0x06, **BTR** (word), **B**lanking **T**ime **R**egister. The value of this register sets the duration of the blanking time for frequency switching in units of 0.1 msec.

BA+0xA, **LER**, **LE**vel **R**egister, it sets the level sense of the *blanking* and *status* input signals of the external PSD. The bit use is as follow:

bit 0, set if the beam switching blanking level is low
bit 1, set if the beam switching status level is low
bit 2, set if the wobbler blanking level is low
bit 3, set if the wobbler status level is low
bit 4, set if the reserve 1 blanking level is low
bit 5, set if the reserve 1 status level is low
bit 6, set if the reserve 2 blanking level is low
bit 7, set if the reserve 2 status level is low
bit 8, set if the reserve 3 blanking level is low
bit 9, set if the reserve 3 status level is low
bit 10, set if the reserve 4 blanking level is low
bit 11, set if the reserve 4 status level is low

BA+0xE, **IDR**, **I**nterrupt **D**uration **R**egister. The value of this register sets the duration of the *Phase Interrupt* and *Status Interrupt*. With the CPU MVME 2401 the scale of times is:

| | | |
|---|---|---|
| 0x1 | for | 1.5 µsec |
| 0x10 | for | 1.6 µsec |
| 0x100 | for | 3.2 µsec |
| 0x200 | for | 4.8 µsec |
| 0x400 | for | 8.3 µsec |
| 0x1000 | for | 28 µsec |

the default value is set to 0x500 with 10 µsec of interrupt duration

BA+0x10, **F11** (longword), frequency 1 of Rx 1

BA+0x14, **F12** (longword), frequency 2 of Rx 1 (frequency switching)

BA+0x18, **F21** (longword), frequency 1 of Rx 2

BA+0x1C, **F22** (longword), frequency 2 of Rx 2 (frequency switching)

BA+0x20, **F31** (longword), frequency 1 of Rx 3

Ba+0x24, **F32** (longword), frequency 2 of Rx 3 (frequency switching)

BA+0x28, **F41** (longword), frequency 1 of Rx 4

BA+0x2C, **F42** (longword), frequency 2 of Rx 4 (frequency switching)

BA+0x200, **FS1** table with the frequencies for Rx1 in case of using the frequency switching in ramp mode. A maximum of 0x80 longwords with 0x80 frequencies could be used (the first and last frequencies in the table must be the initial and final frequencies during the blanking time), then the maximum value for **BTR** is 0x7F (127 frequency steps are possible or what is the same a maximum blanking time of 12.7 msec.).

BA+0x400, **FS2** similar to FS1 but for Rx2

BA+0x600, **FS3** similar to FS1 but for Rx3

BA+0x800, **FS4** similar to FS1 but for Rx4

The registers above and others could be checked (and changed if desired) running the program "/home/penalver/BESYNC/biconf " in the "vac5" system.

**PSDs at the 30m**

The following PSDs are available at the 30m:

Internal generator. This PSD is implemented inside the PSS and it is activated setting the bit 0 of the **STR** register. The cycle has only one phase and the phase time is determined writing de duration into the **PTR** register, the default value for this register is 500 what corresponds to 50 msec. The blanking time is fixed to 0.1 msec. This observing mode is of interest for continuum tracking, continuum on/off measurements and line observation with position switching.

Frequency switching. This PSD is implemented inside the PSS and is activated setting the bit 1 (jump mode) or the bit 2 (ramp mode) of the **STR** register. The cycle has two phases with the same duration and the phase time is determined writing the duration into the **PTR** register. The blanking time is the same for both phases and is determined writing the value into the **BTR** register, the default value for **BTR** is 100 (10 msec.). **PTR** must be bigger than **BTR**, if necessary **PTR** is forced to **PTR=BTR**+1. In the jump mode the frequency is changed in one step at the beginning of the phase. In the ramp mode the frequency is lineally changed during the blanking time, at the rate of one step every 0.1 msec., the maximum permitted value for the BTR is 127 (12.7 msec.) and the corresponding table must be filled with the frequency values during the blanking time (using, for instance, the utility program *freqset*). Frequency switching is available for up to four receivers, with two frequencies of 32 bits per receiver. This observing mode is of interest for line observation. With this PSD are also generated the wobbler simulation output signals: blanking wobbler simul. (a positive pulse during the blanking time) and status wobbler simulator to simulate the output signals from the wobbler system for test purposes without real wobbler operation.

With frequency switching in ramp mode a table of frequencies must be produced with each receiver. The starting value of the table for Rx1 is in RFS1, for Rx2 is in RFS2, and so on. The number of values with each table must be equal to BTR+1 and the initial and final values must correspond to the initial and final frequency. For instance, if **BTR**=5, **F11**=0x04000000 and **F12**=0x04500000, the table for Rx1, starting in RFS1, must contains the sequence

| | | | | | |
|---|---|---|---|---|---|
| F11= 0x04000000 | 0x04100000 | 0x04200000 | 0x04300000 | 0x04400000 | F12= 0x04500000 |

the program */home/penalver/BESYNC/freqset* permits the filling of the tables necessaries for frequency switching in ramp mode.

Beam switching. This PSD is activated setting the bit 3 of the **STR** register. The cycle has four phases with a typical phase time of 57 msec. and blanking time of 33 msec. The sequence of the phases are: sky, blade 1, sky, blade 2. This observing mode is of interest for continuum observations.

Wobbler. This PSD is activated setting the bit 4 of the **STR** register. The cycle has two phases of the same duration determined by the wobbling system. The cycle time is set in the wobbler system between 0.25 and >>1000 sec. The blanking time is determined by the wobbler system itself for any individual phase, it depends on the wobbler throw and typical values are between 50 msec. (20% amplitude) and 110 msec. (100% amplitude). In the PSS the level of the *status* input signal must be inverted setting the bit 3 (0x0008) of the **LER** register. This observing mode is of interest for continuum and line observations.

Other PSDs are also used at the 30m for particular projects as polarimeter, bolometer skydip chopper,… In those cases, depending on the hardware connection, the corresponding bit between 5 and 8 of the **STR** must be set.

Except for frequency switching, with all the others PSD the four frequencies written for the four receivers (F11, F21, F31 and F41) are updated every 100 msec.

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